## REMARKS

Claims 31-42 are pending. Claims 31-40 are presented without further amendment. Claims 41 and 42 are new. No amendments to the specification are made herein.

Claims 31-40 were rejected under the judicially created doctrine of double patenting over claims 15-17 and 20 of U.S. Patent No. 6,678,807. Applicants will file a terminal disclaimer pursuant to 37 CFR §§1.130(b) and 1.312, upon a showing by the Examiner that the claims at issue are otherwise in condition for allowance.

**Rejection of Claims 36 and 40 Under 35 U.S.C. §102(e)**

Claims 36 and 40 have been rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,141,747 to Witt ("Witt"). Applicants respectfully traverse the Examiner's rejection because *Witt* does not teach or suggest all of the elements of the claims. Specifically, *Witt* does not teach a processor having a write combining buffer, where the processor authorizes store buffer forwarding by determining that: (1) the memory region associated with a load instruction matches a cache line address; and (2) the memory associated with store instructions completely covers the memory region associated with the load instruction. These two steps ensure that store buffer forwarding will be authorized only when the relevant data will be transmitted to memory in a single atomic transaction, thereby ensuring data consistency in a multiprocessor environment. *Witt* overlooks the critical need to guarantee an atomic update of system memory in a multiprocessor architecture and *Witt* therefore fails to determine whether these two criteria are satisfied before permitting store-forwarding to occur.

In the Office Action, the Examiner indicated that *Witt* anticipates claims 36 and 40 because "[l]oad data may be forwarded from the store queue if the load data is stored therein, *which relates to the determining step as claimed* [col. 2, lines 12-14; here the matching of first and second memory regions is contemplated, and the covering of the second step by the first is realized and produces the forwarding of data as claimed]." Office Action at 5 (emphasis added). The Applicants respectfully disagree. Rather than teach or suggest the determining steps as claimed, *Witt* merely describes forwarding the load data *if it is available*. *See, e.g.*, col. 2, lines 12-14 ("the load data may be forwarded from the store queue if the load data is stored therein").

Importantly, when *Witt* performs store-forwarding, no steps are taken to ensure that all of the relevant store operations will become globally observed (GO) at the same time. Thus, in contrast to the present invention, *Witt* will not operate properly in a multi-processor architecture. Even though *Witt* states that his invention could be implemented in a multiprocessor environment (as the Examiner points out), *Witt* makes no provision to ensure that the results of a store-forwarded load operation, as executed by one of several processors, will yield predictable results when the forwarded data is supplied by a plurality of pending store operations.

The present application provides examples illustrating the erroneous behavior of store-forwarding operations in architectures similar to that of *Witt*. Summarizing those examples, if a given load operation is satisfied by store-forwarding from two different store operations, unpredictable results may occur in a multiprocessor environment if those two store operations are globally observed at different times. The present invention solves that problem, which *Witt* overlooks, by ensuring that the memory requested by a load instruction matches a cache line address, and by further requiring the memory requested by a load instruction to be completely covered by memory associated with the store instructions from which the desired load data will be forwarded.

For at least these reasons, Applicants respectfully assert that *Witt* does not teach or suggest the invention described by claims 36 and 40. As a result, *Witt* does not anticipate these claims. Accordingly, Applicants respectfully request withdrawal of these grounds of rejection.

**Rejection of Claims 31 and 35 Under 35 U.S.C. §103(a)**

Claims 31 and 35 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over *Witt* in view of Tanenbaum. Applicants respectfully traverse the Examiner's rejection. Claims 31 and 35 both show a store buffer forwarding apparatus having instructions to determine that: (1) the memory region associated with a load instruction matches a cache line address; and (2) the memory associated with previous store instructions completely covers the memory region associated with the load instruction. As explained above, these two steps ensure that store buffer forwarding will be authorized only when the relevant data will be transmitted to memory in a single atomic transaction, thereby ensuring data consistency in a multiprocessor environment. *Witt* fails to teach or suggest these features.

*Tanenbaum*, according to the Examiner, teaches that computer hardware capabilities can be reproduced in software, and thus it would have been obvious to one skilled in the art to construct a software version of *Witt's* store-forwarding system. However, without disputing the Examiner's use of *Tanenbaum*, even if *Witt's* store-forwarding system were realized in software using *Tanenbaum* as a guide, the result still would not disclose the claimed invention. Nothing in either *Witt* or *Tanenbaum* discloses steps or features to ensure that store buffer forwarding will be authorized only when the relevant data will be transmitted to memory in a single atomic transaction. In particular, nothing in a *Witt-Tanenbaum* combination would teach or suggest store buffer forwarding only when the memory region associated with a load instruction matches a cache line address and when the memory associated with the relevant store instructions completely covers the memory region associated with the load instruction.

For at least these reasons, Applicants respectfully assert that claims 31 and 35 are patentable over *Witt* in view of *Tanenbaum*. Accordingly, Applicants respectfully request withdrawal of these grounds of rejection.

**Claims 32-34 and 37-39 are Patentable Over the Cited References**

In the Office Action, the Examiner rejected all of the pending claims, but discussed only claims 31, 35, 36 and 40 in the context of *Witt* and *Tanenbaum*. Presumably, therefore, claims 32-34 and 37-39 are allowable over these references and the only remaining issue is the double patenting rejection with respect to U.S. Patent No. 6,678,807. As stated above, Applicants will file a terminal disclaimer pursuant to 37 CFR §§1.130(b) and 1.312, upon a showing by the Examiner that these claims are otherwise in condition for allowance.

**New Claims 41-42 are Patentable Over the Cited References**

Claims 41 and 42 have been added to the application. Applicants respectfully submit that claims 41 and 42 are patentable over the cited references because they disclose a comparison circuit that generates a signal indicating that store buffer forwarding is authorized if the memory region requested by a load operation can be globally observed in a single atomic transaction and if store data in a write combining buffer (WCB) completely covers the memory region requested by the load operation. The cited references neither teach nor suggest this kind of comparison

circuit. Accordingly, claims 41 and 42 are patentable over the cited references and should be allowed.

**Conclusion**

In view of the above amendments and remarks, the Applicants respectfully submit that the present application is now in condition for allowance. A timely Notice to that effect is earnestly solicited. The Examiner is invited to contact the undersigned at (202) 220-4200 to discuss any aspect of the application.

Respectfully submitted,

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